wherein, when a cross-section on a side of said first channel is S1, a cross-section on a side of said first gate electrode is S2, a cross-section on a side of said second channel is S3, and a cross-section on a side of said second gate insulation film is S4, a condition of:

$$S2/S1 > S4/S3$$

is satisfied, and

an area of a bottom part of said first gate electrode is larger than an area of an upper part of said first gate insulation film, and an area of a bottom part of said second gate electrode is larger than an area of an upper part of said second gate insulation film.

B2 Cont.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are pending in the present application with Claims 1, 9 and 10 having been amended by the present amendment.

In the outstanding Office Action, Claims 1, 2 and 4-9 were rejected under 35 U.S.C. § 102(e) as anticipated by Krivokapic et al; Claims 3, 10 and 11 were rejected under 35 U.S.C. § 103(a) as unpatentable over Krivokapic et al; and Claim 12 was indicated as allowable if rewritten in independent form.

Applicants thank the Examiner for the indication for the allowable subject matter.

Claims 1, 2 and 4-9 stand rejected under 35 U.S.C. § 102(e) as anticipated by Krivokapic et al. This rejection is respectfully traversed.

Claim 1 has been amended to recite that when a first area of the gate insulating film adjacent to the electrode is S1, a second area of the gate insulating film adjacent to the channel is S2, and a third area of a bottom part of the gate electrode is S3, the area S1 is

larger than the area S2, the area S3 is larger than the area S1, a part of the third area S3 is connected to the gate insulating film, and the other part of the third area S3 is not connected to the gate insulating film. Independent Claim 9 has been similarly amended to recite that an area of a bottom part of the gate electrode is larger than an area of an upper part of the gate insulating film.

In a non-limited example, Figure 22H shows that the area of the bottom part of the gate electrode 15 is larger than the area of the upper part of the gate insulating film 14 (or the upper part of the gate insulating film 14 is smaller than the lower part of the gate electrode 15). With this configuration, the channel region, the source, drain, element isolation and gate contacting regions of the semiconductor device can be widened (see the comparison of prior art Figure 12A and Applicants' Figure 12C).

The outstanding Office Action states Krivokapic et al teach the claimed invention and cites Figure 20. However, as shown in Figure 20, the area of the bottom part of the gate electrode 220 is the same as an area of the upper part of the gate insulating film 210. Therefore, the device in Krivokapic et al does not achieve the same advantages as the claimed invention.

Accordingly, it is respectfully submitted independent Claims 1 and 9 and each of the claims depending therefrom are allowable.

Claims 3, 10 and 11 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Krivokapic et al. This rejection is respectfully traversed.

Claim 3 depends on Claim 1, which as discussed above is believed to be allowable. Further, independent Claim 10 includes similar features to that discussed above. That is, independent Claim 10 recites that the area of the bottom part of the first gate electrode is larger than an area of the upper part of the first gate insulating film, and the area of the

bottom part of the second gate electrode is larger than an area of the upper part of the second gate insulating film. As discussed above, Krivokapic et al do not teach or suggest these features. Accordingly, it is respectfully submitted independent Claim 10 and dependent Claim 11 are also allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

--1. (Twice Amended) A semiconductor device comprising:

a channel of a first conductivity type formed on a surface layer of a semiconductor substrate;

a source and a drain of a second conductivity type formed on both sides of the channel;

a gate insulation film with a first relative permittivity formed at least on said channel directly or through a buffer insulation film;

a gate electrode formed on said gate insulation film; and

a side insulation film formed at least on a side of said gate insulation film and having a second relative permittivity which is smaller than the first relative permittivity, wherein

when a first area of said gate insulation film[, the first area being] adjacent to said gate electrode[,] is [S_1, and] S1, a second area [thereof, the second area being] of said gate insulating film adjacent to said channel[,] is S2, and a third area of a bottom part of said gate electrode is S3,

the area S1 is larger than the area S2, the area S3 [and an area of a bottom part of said gate electrode in contact with the gate insulation film] is larger than the area S1, a part of the

third area S3 is connected to said gate insulating film, and the other part of the third area S3 is not connected to said gate insulating film.

9. (Twice Amended) A semiconductor device comprising:

a channel of a first conductivity type formed on a surface layer of a semiconductor substrate;

a source and a drain of a second conductivity type formed on both sides of the channel;

a gate insulation film with a first relative permittvity formed at least on said channel directly or through a buffer insulation film;

a gate electrode formed on said gate insulation film; and

a side insulation film formed at least on a side of said gate insulation film and having a second relative permittvity which is smaller than the first relative permittivity,

wherein an electric flux density in said gate insulation film on a side towards the channel side is more dense than an electric flux density in said gate insulation film on a side towards the gate electrode, and an area of a bottom part of said gate electrode [in contact with the gate insulation film] is larger than an area of an upper part of said gate insulation film.

10. (Twice Amended) A semiconductor device comprising:

a plurality of first MOS transistors, each of said first MOS transistors including,

a first channel of a first conductivity type formed on a surface layer of a semiconductor substrate,

a first source and a first drain of a second conductivity type formed to both sides of said first channel,

a first gate insulation film with a first relative permittivity formed at least on the first channel directly or through a buffer insulation film,

a first gate electrode formed on said first gate insulation film, and

a first side insulation film formed at least on side of said first gate insulation film and having a second relative permittivity which is smaller than the first relative permittvity; and

a plurality of second MOS transistors, each of said second MOS transistors including,

a second channel of the first conductivity type formed on a surface layer of said substrate,

a second source and a second drain of the second conductivity type formed on both sides of said second channel,

a second gate insulation film with the first relative permittvity formed at least on said second channel directly or through a buffer insulation film,

a second gate electrode formed on said second gate insulation film, and

a second side insulation film formed at least on side of said second gate insulation film and having said second relative permittvity,

wherein, when a cross-section on a side of said first channel is S1, a cross-section on a side of said first gate electrode is S2, a cross-section on a side of said second channel is S3, and a cross-section on a side of said second gate insulation film is S4, a condition of:

$S2/S1 > S4/S3$

is satisfied, and

an area of a bottom part of said first gate electrode [in contact with the first gate insulation film] is larger than an area of an upper part of said first gate insulation film, and an area of a bottom part of said second gate electrode [in contact with the second gate insulation film] is larger than an area of an upper part of said second gate insulation film.--